

# 512K x 16 Static RAM

## Features

- **Temperature Ranges**
  - Automotive-A: -40°C to 85°C
  - Automotive-E: -40°C to 125°C
- **Voltage range:**
  - CY62157CV30: 2.7V–3.3V
  - CY62157CV33: 3.0V–3.6V
- **Ultra-low active power**
  - Typical active current: 1.5 mA @ f = 1 MHz
  - Typical active current: 5.5 mA @ f = f<sub>max</sub>
- **Low standby power**
- **Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$  and  $\overline{OE}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in Pb-free and non Pb-free 48-ball FBGA package**

## Functional Description<sup>[1]</sup>

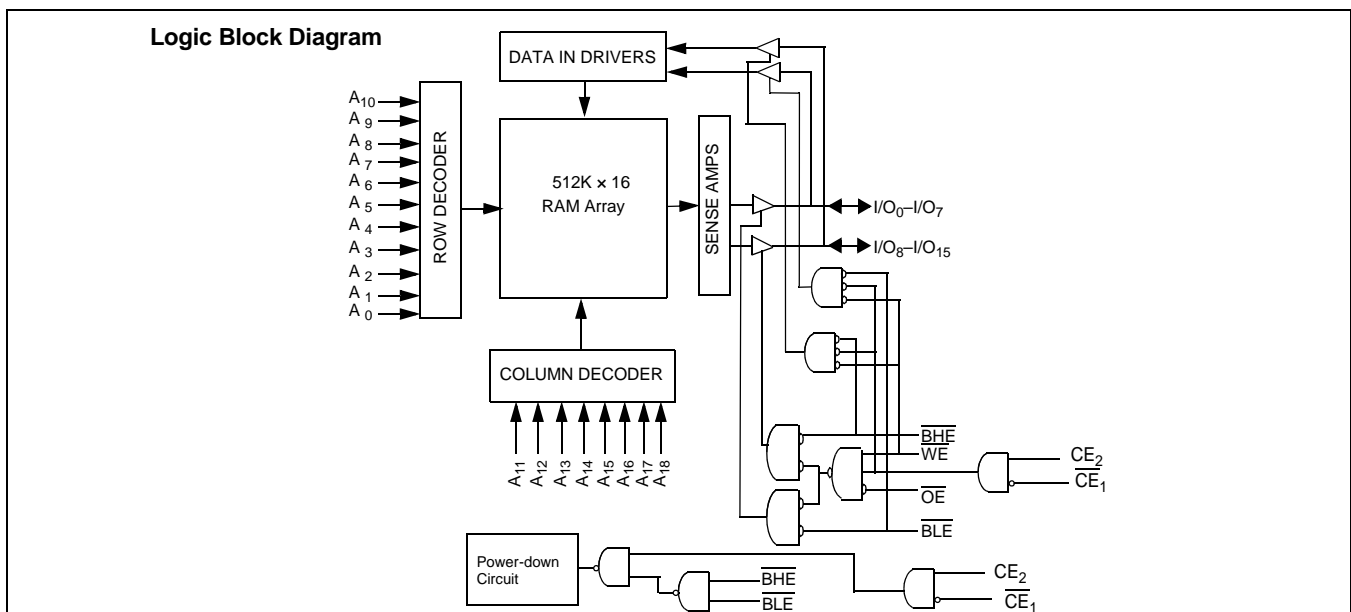
The CY62157CV30/33 are high-performance CMOS static RAMs organized as 512K words by 16 bits. These devices feature advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The devices also have an automatic power-down feature that

significantly reduces power consumption by 80% when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW or both BLE and BHE are HIGH). The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when: deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a write operation ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH and WE LOW).

Writing to the device is accomplished by taking Chip Enable 1 ( $\overline{CE}_1$ ) and Write Enable (WE) inputs LOW and Chip Enable 2 ( $CE_2$ ) HIGH. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>).

Reading from the device is accomplished by taking Chip Enable 1 ( $\overline{CE}_1$ ) and Output Enable ( $\overline{OE}$ ) LOW and Chip Enable 2 ( $CE_2$ ) HIGH while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.

The CY62157CV30/33 are available in a 48-ball FBGA package.



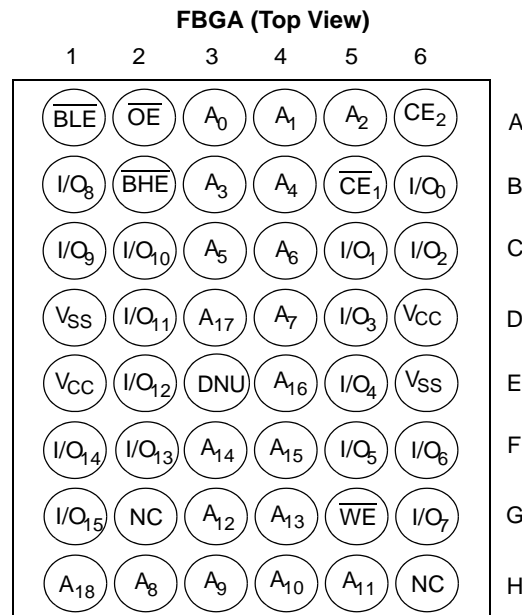
**Note:**

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

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**Product Portfolio**

Product	Range	V <sub>CC</sub> Range			Power Dissipation					
					Operating (I <sub>CC</sub> ) mA				Standby (I <sub>SB2</sub> ) μA	
		Min.	Typ. <sup>[2]</sup>	Max.	f = 1 MHz		f = f <sub>max</sub>		Typ. <sup>[2]</sup>	Max.
CY62157CV30	Automotive-E	2.7V	3.0V	3.3V	1.5	3	7	15	8	70
CY62157CV33	Automotive-A	3.0V	3.3V	3.6V	1.5	3	5.5	12	10	30
	Automotive-E				1.5	3	7	15	10	80

**Pin Configurations<sup>[2, 3, 4]</sup>**

**Pin Definitions**

Name	Definition
Input	<b>A<sub>0</sub>-A<sub>18</sub></b> . Address Inputs
Input/Output	<b>I/O<sub>0</sub>-I/O<sub>15</sub></b> . Data lines. Used as input or output lines depending on operation
Input/Control	<b>WE</b> . Write Enable, Active LOW. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
Input/Control	<b>CE<sub>1</sub></b> . Chip Enable 1, Active LOW.
Input/Control	<b>CE<sub>2</sub></b> . Chip Enable 2, Active HIGH.
Input/Control	<b>OE</b> . Output Enable, Active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins
Ground	<b>V<sub>SS</sub></b> . Ground for the device
Power Supply	<b>V<sub>CC</sub></b> . Power supply for the device

**Notes:**

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.
3. NC pins are not connected on the die.
4. E3 (DNU) can be left as NC or V<sub>SS</sub> to ensure proper application.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied.....-55°C to +125°C  
 Supply Voltage to Ground Potential ...-0.5V to  $V_{CCmax} + 0.5V$   
 DC Voltage Applied to Outputs in High-Z State<sup>[5]</sup>.....-0.5V to  $V_{CC} + 0.3V$   
 DC Input Voltage<sup>[5]</sup>.....-0.5V to  $V_{CC} + 0.3V$   
 Output Current into Outputs (LOW) .....20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

**Operating Range**

Device	Range	Ambient Temperature [T <sub>A</sub> ] <sup>[6]</sup>	V <sub>CC</sub>
CY62157CV30	Automotive-E	-40°C to +125°C	2.7V – 3.3V
CY62157CV33	Automotive-A	-40°C to +85°C	3.0V – 3.6V
	Automotive-E	-40°C to +125°C	

**Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions	CY62157CV30-70			Unit
			Min.	Typ. <sup>[2]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA V <sub>CC</sub> = 2.7V	2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA V <sub>CC</sub> = 2.7V			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2		V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage		-0.3		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10		+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-10		+10	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		7	15	mA
		f = 1 MHz				
I <sub>SB1</sub>	Automatic CE Power-Down Current— CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = f <sub>max</sub> (Address and Data Only), f = 0 (OE, WE, BHE and BLE)		8	70	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.3V		8	70	μA

**Notes:**

- V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns.
- T<sub>A</sub> is the "Instant-On" case temperature.

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**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	CY62157CV33-70			Unit	
			Min.	Typ. <sup>[2]</sup>	Max.		
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA V <sub>CC</sub> = 3.0V	2.4			V	
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA V <sub>CC</sub> = 3.0V			0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2.2		V <sub>CC</sub> + 0.3V	V	
V <sub>IL</sub>	Input LOW Voltage		-0.3		0.8	V	
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	Auto-A	-1	+1	μA	
			Auto-E	-10	+10	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	Auto-A	-1	+1	μA	
			Auto-E	-10	+10	μA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = 3.6V I <sub>OUT</sub> = 0 mA CMOS Levels	Auto-A	5.5	12	mA
		f = 1 MHz		Auto-E	7	15	
				Auto-A/ Auto-E	1.5	3	
I <sub>SB1</sub>	Automatic CE Power-Down Current—CMOS Inputs	CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V or CE <sub>2</sub> ≤ 0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = f <sub>max</sub> (Address and Data Only), f = 0 (OE, WE, BHE, and BLE)	Auto-A	10	30	μA	
			Auto-E	10	80	μA	
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2V or CE <sub>2</sub> ≤ 0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.6V	Auto-A	10	30	μA	
			Auto-E	10	80	μA	

**Thermal Resistance<sup>[7]</sup>**

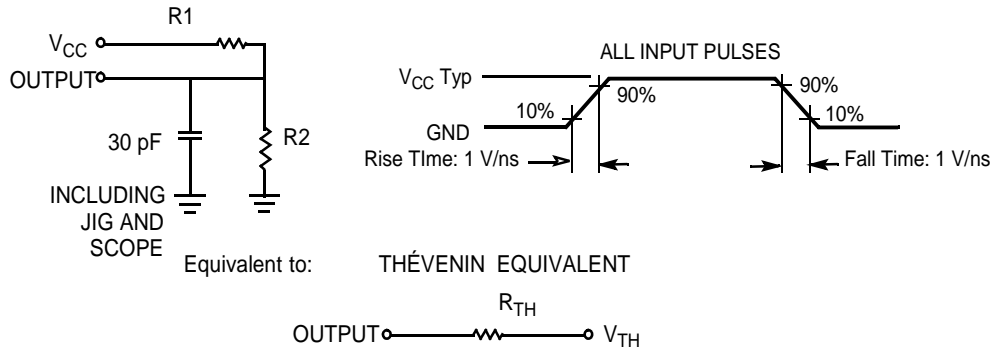
Parameter	Description	Test Conditions	FBGA	Unit
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	55	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		16	°C/W

**Note:**

7. Tested initially and after any design or process changes that may affect these parameters.

**Capacitance<sup>[7]</sup>**

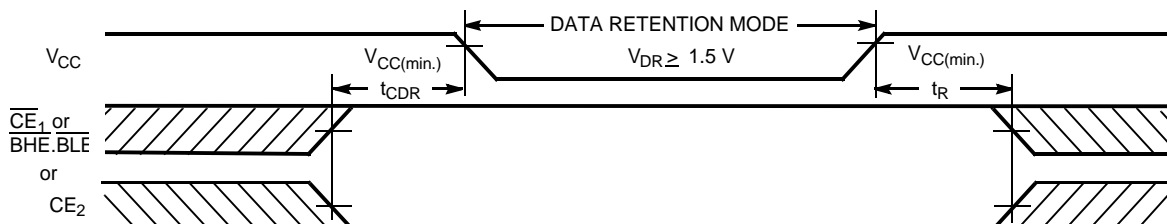
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ.)</sub>	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**AC Test Loads and Waveforms**


Parameters	3.0V	3.3V	Unit
R1	1.105	1.216	KΩ
R2	1.550	1.374	KΩ
R <sub>TH</sub>	0.645	0.645	KΩ
V <sub>TH</sub>	1.75	1.75	V

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions	Min.	Typ. <sup>[2]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.5			V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.5V, $\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V	Auto-A	4	20	μA
			Auto-E	4	60	μA
t <sub>CDR</sub> <sup>[8]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[8]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

**Data Retention Waveform<sup>[9]</sup>**

**Notes:**

8. Full Device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> > 100 μs or stable at V<sub>CC(min.)</sub> > 100 μs.

9. BHE.BLE is the AND of both BHE and BLE. Chip can be deselected by either disabling the chip enable signals or by disabling both BHE and BLE.

**Switching Characteristics** Over the Operating Range <sup>[10]</sup>

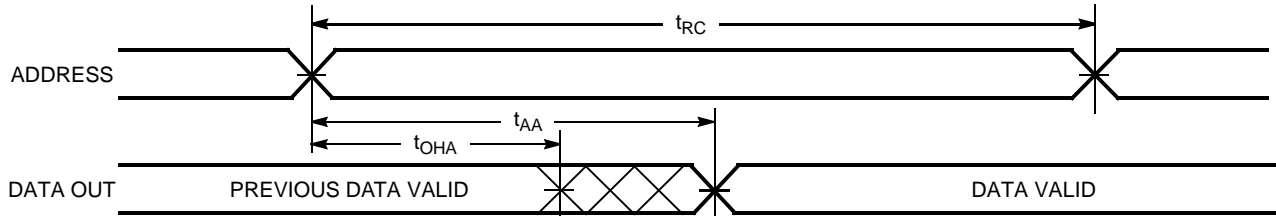
Parameter	Description	70 ns		Unit
		Min.	Max.	
<b>Read Cycle</b>				
$t_{RC}$	Read Cycle Time	70		ns
$t_{AA}$	Address to Data Valid		70	ns
$t_{OHA}$	Data Hold from Address Change	10		ns
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Data Valid		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low-Z <sup>[11]</sup>	5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High-Z <sup>[11, 12]</sup>		25	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Low-Z <sup>[11]</sup>	10		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH or $CE_2$ LOW to High-Z <sup>[11, 12]</sup>		25	ns
$t_{PU}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Power-up	0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH or $CE_2$ LOW to Power-down		70	ns
$t_{DBE}$	$\overline{BHE}/\overline{BLE}$ LOW to Data Valid		70	ns
$t_{LZBE}^{[11]}$	$\overline{BHE}/\overline{BLE}$ LOW to Low-Z <sup>[13]</sup>	5		ns
$t_{HZBE}$	$\overline{BHE}/\overline{BLE}$ HIGH to High-Z <sup>[11, 12]</sup>		25	ns
<b>Write Cycle<sup>[14]</sup></b>				
$t_{WC}$	Write Cycle Time	70		ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Write End	60		ns
$t_{AW}$	Address Set-up to Write End	60		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	50		ns
$t_{BW}$	$\overline{BHE}/\overline{BLE}$ Pulse Width	60		ns
$t_{SD}$	Data Set-up to Write End	30		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[11, 12]</sup>		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[11]</sup>	5		ns

**Notes:**

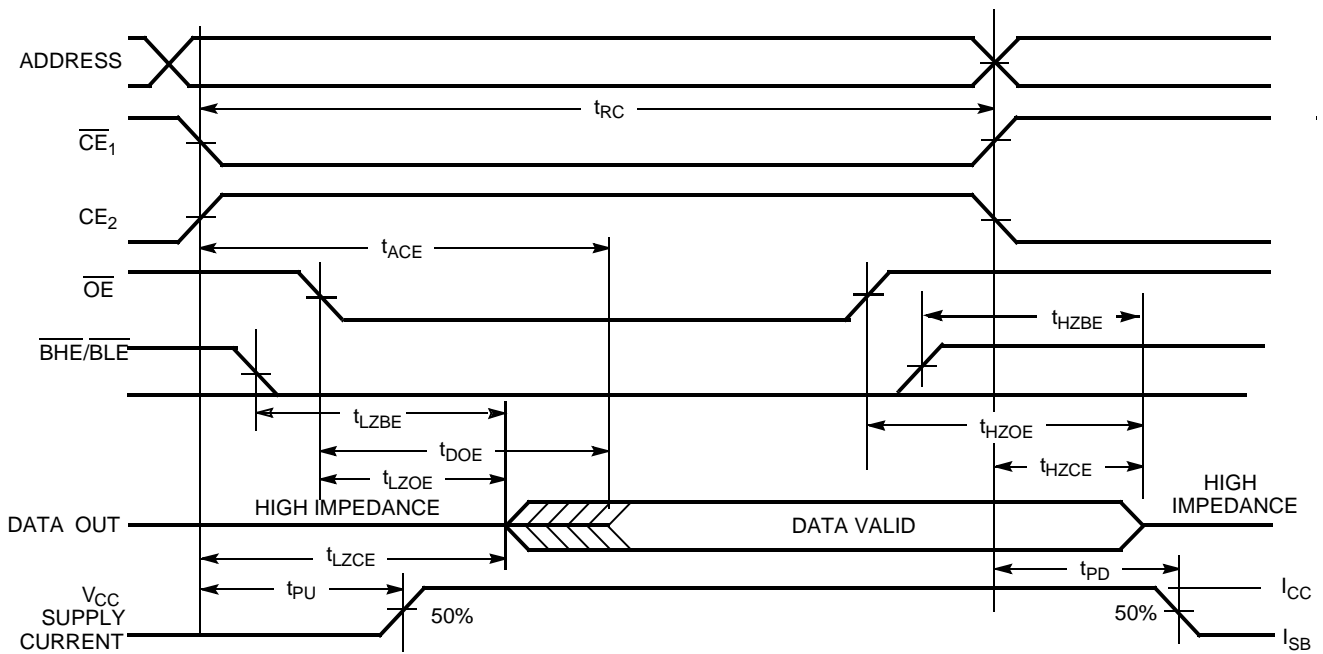
10. Test conditions assume signal transition time of 5 ns or less, timing reference levels of  $V_{CC(typ.)}/2$ , input pulse levels of 0 to  $V_{CC(typ.)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
11. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
12.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
13. When both byte enables are toggled together this value is 10 ns.
14. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ ,  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a Write and any of these signals can terminate a Write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the Write.

### Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled)<sup>[15, 16]</sup>



Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[16, 17]</sup>



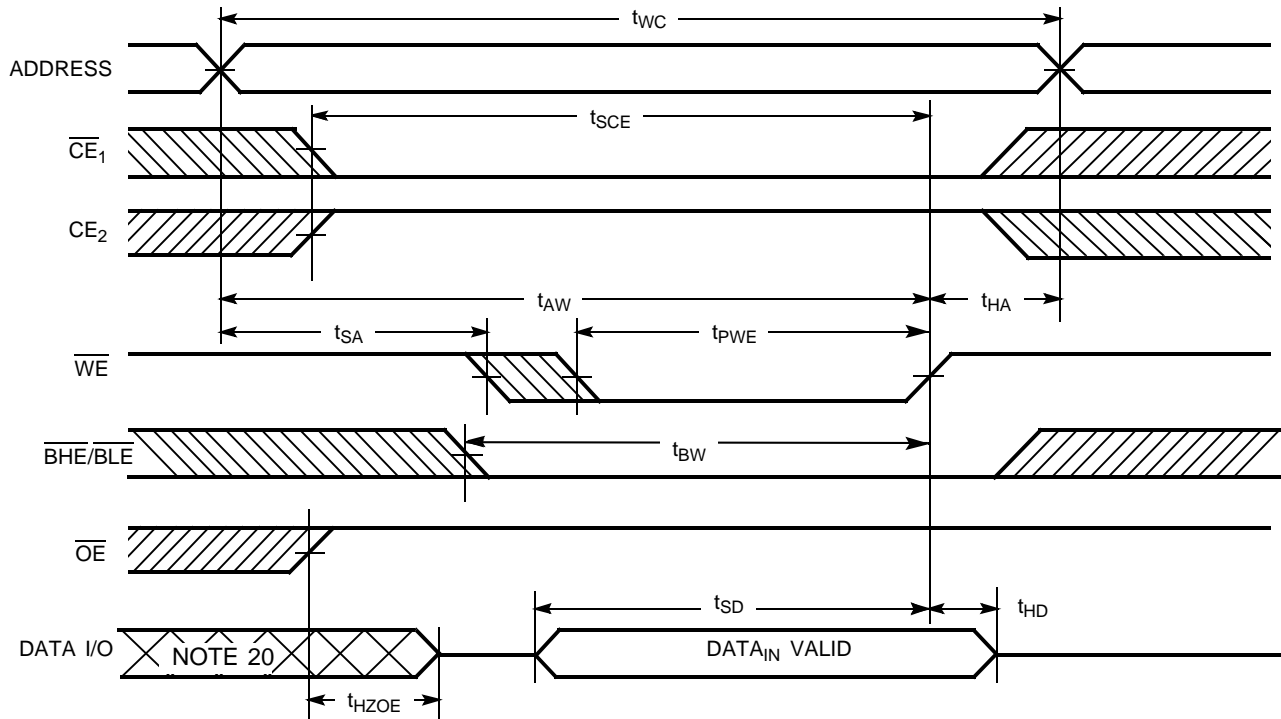
**Notes:**

- 15. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ ,  $CE_2 = V_{IH}$ .
- 16. WE is HIGH for Read cycle.
- 17. Address valid prior to or coincident with  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $CE_2$  transition HIGH.

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Switching Waveforms (continued)

Write Cycle No. 1 (WE Controlled)<sup>[14, 18, 19]</sup>



Notes:

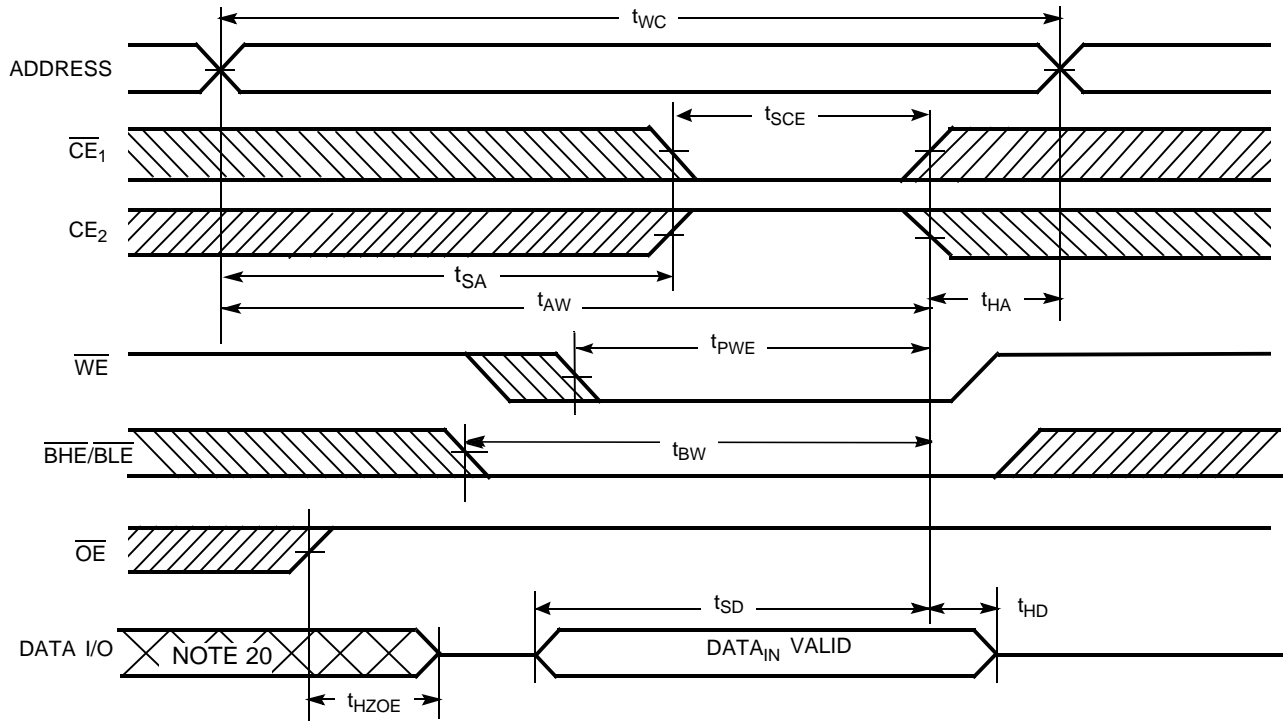
- 18. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
- 19. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
- 20. During this period, the I/Os are in output state and input signals should not be applied.

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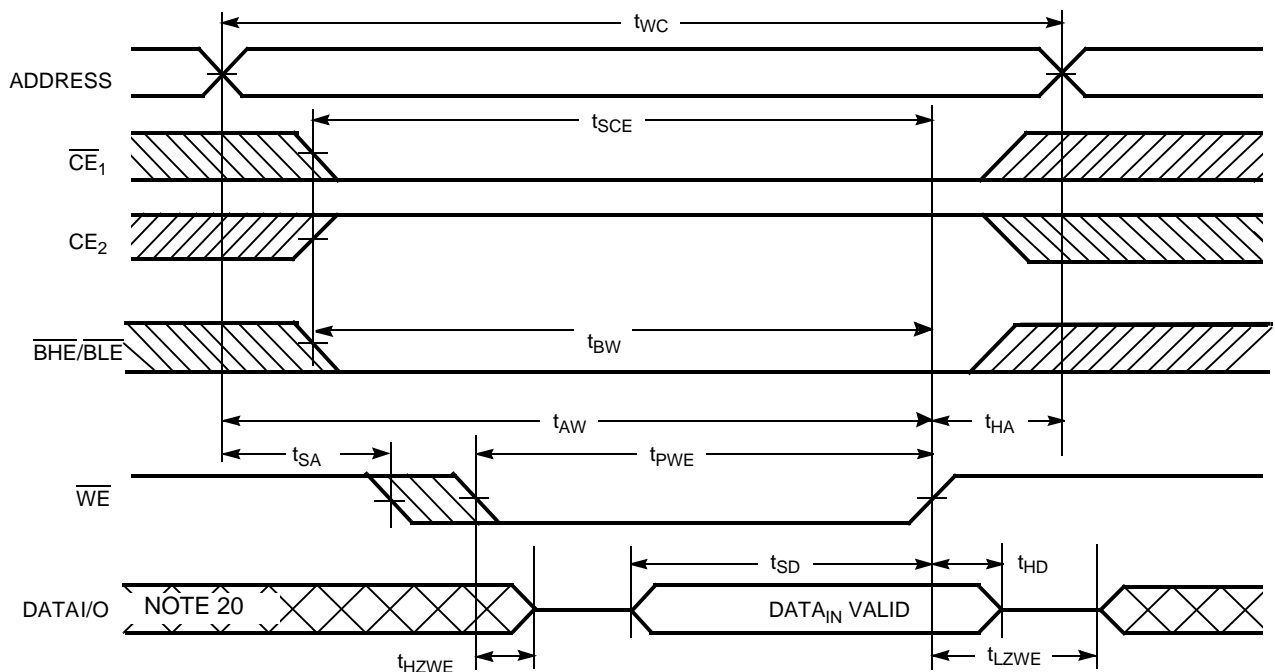


Switching Waveforms (continued)

Write Cycle No. 2 ( $\overline{CE}_1$  or  $CE_2$  Controlled) [14, 18, 19]



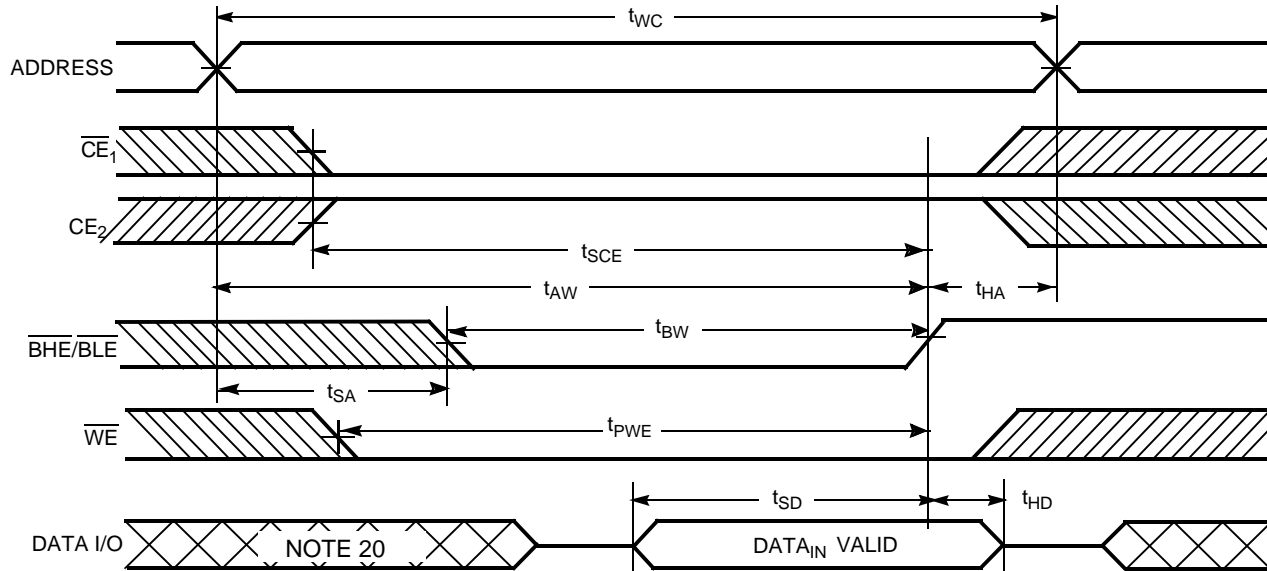
Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [19]



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Switching Waveforms (continued)

Write Cycle No. 4 (BHE/BLE Controlled, OE LOW)<sup>[19]</sup>



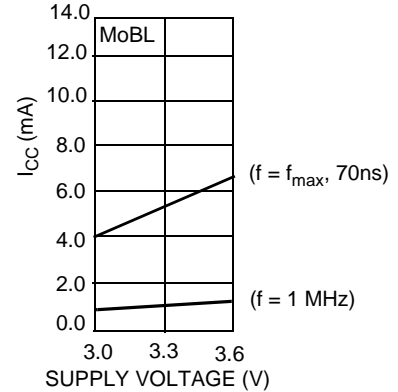
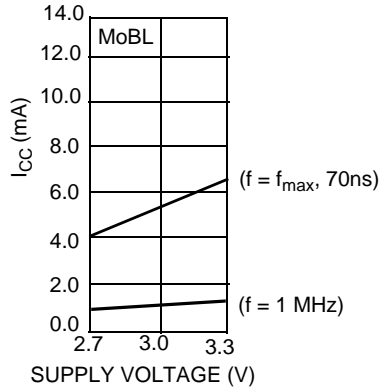
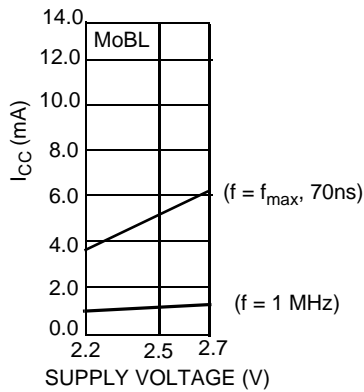
Truth Table

CE <sub>1</sub>	CE <sub>2</sub>	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
L	H	H	L	L	L	Data Out (I/O <sub>0</sub> -I/O <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	H	H	L	H	L	Data Out (I/O <sub>0</sub> -I/O <sub>7</sub> ); I/O <sub>8</sub> -I/O <sub>15</sub> in High Z	Read	Active (I <sub>CC</sub> )
L	H	H	L	L	H	Data Out (I/O <sub>8</sub> -I/O <sub>15</sub> ); I/O <sub>0</sub> -I/O <sub>7</sub> in High Z	Read	Active (I <sub>CC</sub> )
L	H	H	H	L	L	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	H	H	H	L	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	H	H	L	H	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	L	X	L	L	Data In (I/O <sub>0</sub> -I/O <sub>15</sub> )	Write	Active (I <sub>CC</sub> )
L	H	L	X	H	L	Data In (I/O <sub>0</sub> -I/O <sub>7</sub> ); I/O <sub>8</sub> -I/O <sub>15</sub> in High Z	Write	Active (I <sub>CC</sub> )
L	H	L	X	L	H	Data In (I/O <sub>8</sub> -I/O <sub>15</sub> ); I/O <sub>0</sub> -I/O <sub>7</sub> in High Z	Write	Active (I <sub>CC</sub> )

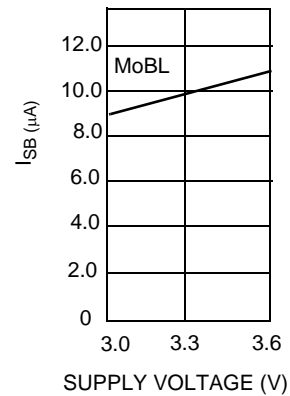
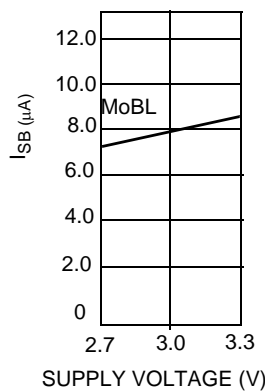
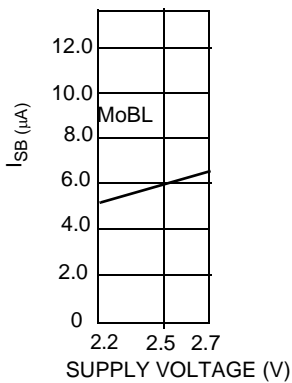
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Typical DC and AC Characteristics<sup>[2]</sup>

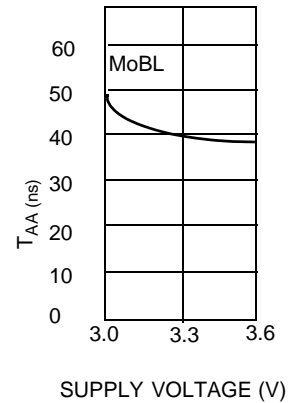
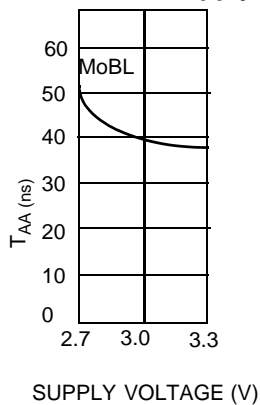
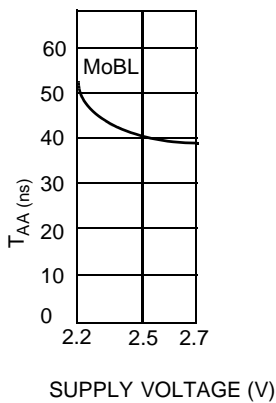
**Operating Current vs. Supply Voltage**



**Standby Current vs. Supply Voltage**



**Access Time vs. Supply Voltage**



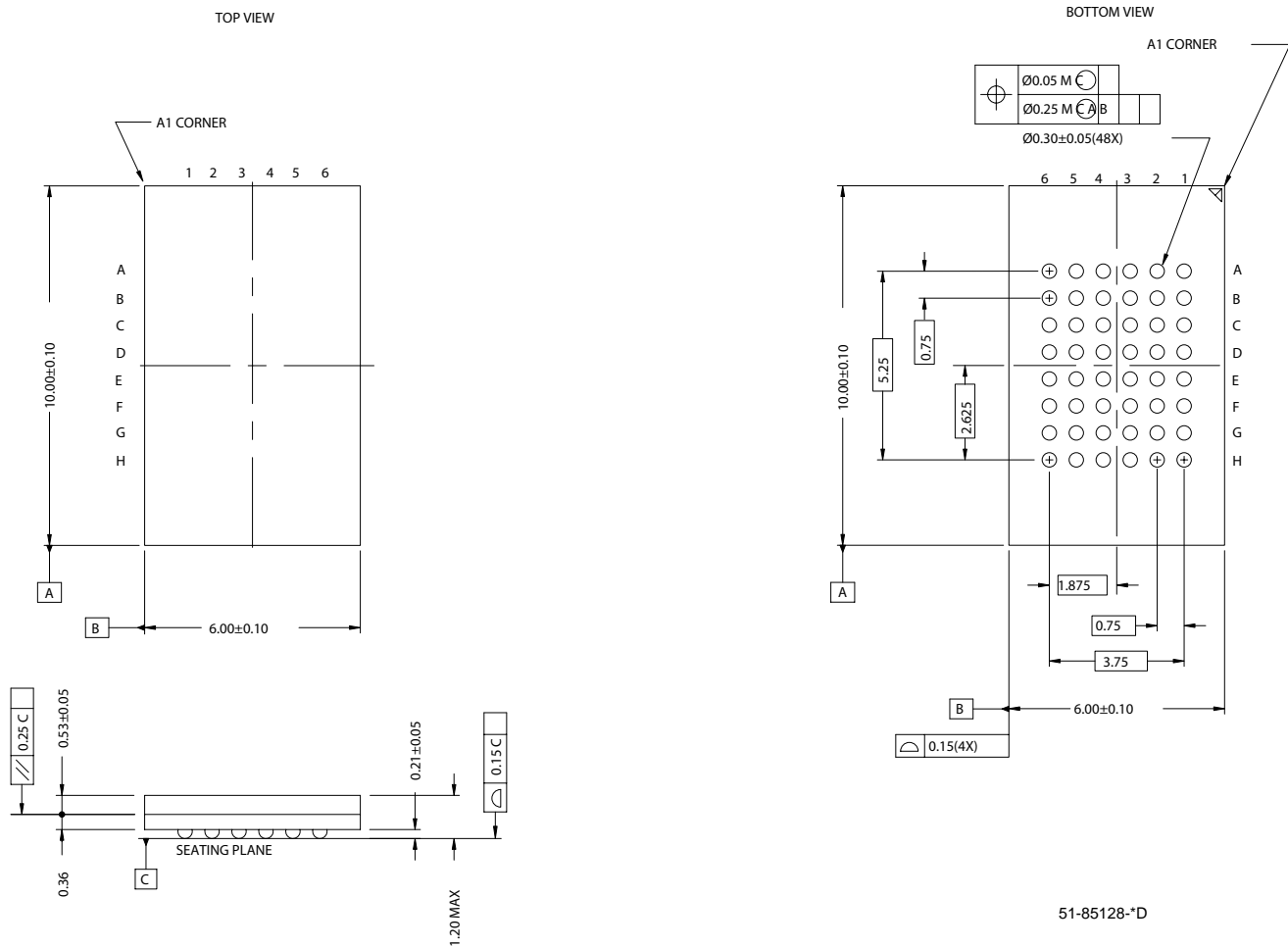
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**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62157CV30LL-70BAE	51-85128	48-Ball (6 mm x 10 mm x 1.2 mm) FBGA	Automotive-E
	CY62157CV33LL-70BAXA			Automotive-A
	CY62157CV33LL-70BAE			Automotive-E

**Package Diagram**

**48-Ball (6 mm x 10 mm x 1.2 mm) FBGA (51-85128)**



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**Document History Page**

Document Title: CY62157CV30/33 512K x 16 Static RAM Document Number: 38-05014				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106184	05/10/01	HRT/MGN	New data sheet – Advance Information
*A	107241	07/24/01	MGN	Made corrections to Advance Information Added 55 ns bin
*B	109621	03/11/02	MGN	Changed from Advance Information to Final
*C	114218	05/01/02	GUG/MGN	Improved Typical and Max I <sub>CC</sub> values
*D	238448	See ECN	AJU	Added Automotive Product Information
*E	269729	See ECN	SYT	Added Automotive Product information for CY62157CV30 – 70 ns Added I <sub>IX</sub> and I <sub>OZ</sub> values for Automotive range of CY62157CV33 – 70 ns
*F	498575	See ECN	NXR	Removed Industrial Operating Range Removed 55 ns speed bin Removed CY62157CV25 part number from the Product Offering Added Automotive-A operating range Updated the Ordering Information Table

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